ABSTRACT OF THE DISCLOSURE

Various embodiments of methods and systems for implementing a return address prediction mechanism in a microprocessor are disclosed. In one embodiment, a return

5   address prediction mechanism includes a return storage and a controller. The return storage includes one or more entries. One of the entries includes a count and a first return address that corresponds to a recently detected call operation. The controller is configured to receive a new return address that corresponds to a call instruction and to compare the new return address to the return address stored in the entry. If the new

10   return address equals the return address in the entry, the controller may be configured to increase the value of the count in the entry. By increasing the count instead of allocating a new entry in the return storage to the new return address, the effective size of the return storage may be increased.

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